IDS #0304

| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | | | | Application Number | 10/624,794 |
|---|---|---|---|---|---|
| | | | | Filing Date | July 22, 2003 |
| | | | | First Named Inventor | Juha Mikko Hakkarainen |
| | | | | Art Unit | ~~Unassigned~~ 2826 |
| | | | | Examiner Name | ~~Unassigned~~ Pert |
| Sheet | 1 | of | 2 | Attorney Docket Number | 55123P256 |

| NON PATENT LITERATURE DOCUMENTS | | | |
|---|---|---|---|
| Examiner Initials* | Cite No.[1] | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T[2] |
| EP | | BEHZAD RAZAVI, Design of Analog CMOS Integrated Circuits, pgs. 619-627, 637-462 and 650-653, McGraw-Hill Higher Education, ISBM 0071188150, 2001. | |
| EP | | IURI MEHR & LARRY SINGER, A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC, pgs. 318-325, IEEE Journal of Solid-State Circuits, Vol. 35 No. 3, March 2002. | |
| EP | | Lessons in Electrical Circuits, Vol IV (Digital), Chapter 13, http://www.ibiblio.org/obp/elecrticalcircuits/digital/digi_13.html, 4/2003. | |
| EP | | B.RAZAVI & B.WOOLEY, A 12-b 5-MSample/s Two-Step CMOS A/D Converter, IEEE Journal of Solid-State Circuits, pgs. 1667-1678, Vol. 27 No. 12, December 1992. | |
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| EP | | D.ALLSTOT & W.BLACK, Technologyical Design Considerations for Monolithic MOS Switched-Capacitor Filtering Systems, pgs 967-986, Prod. of the IEEE, Vol 71 No 8, August 1983. | |
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| Examiner Signature | Eun Pert | Date Considered | 4-2-06 |
|---|---|---|---|

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

[1]Applicant's unique citation designation number. [2]Applicant is to place a check mark here if English language Translation is attached.

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| Sheet | 2 | of | 2 |
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|---|---|---|---|
| EP | | YANNIS TSIVIDIS & PAOLO ANTOGNETTI, Design of MOS VLSI Circuits for Telecommunications, pgs. 20-22, 314-333, Prentice-Hall, New Jersey, ISBN 013200643X01, 1985. | |
| EP | | PAUL R. GRAY & ROBERT G. MEYER, Analysis and Design of Analog Integrated Circuits, Third Edition, pgs. 139-140, 167-170, John Wiley & Sons, Inc., ISBN 0471574953, 1993. | |
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| EP | | YOUNG-DEUK JEON, SEUNG-CHUL LEE, SANG-MIN YOO, & SEUNG-HOON LEE, Acquisition-Time Minimization and Merged-Capacitor Switching Techniques for Sampling-Rate and Resoulution Improvement of CMOS ADCs, pgs. 451-454, 2000 IEEE International Symposium on Circuits and Systems, 5/28-31, Geneva, Switzerland, 2000. | |
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| Examiner Signature | Evan Pert | Date Considered | 4-2-06 |
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